Claims

What is claimed is:

1. A method for improving a photolithographic patterning process in a dual damascene process comprising the steps of:

providing at least one via opening extending through a thickness of layers sequentially including a dielectric anti-reflectance layer (DARC), a hard mask layer, and an insulating layer said via opening in closed communication with a conductive region underlying the insulating layer;

forming a resinous layer over the DARC layer to include filling the at least one via opening;

removing the resinous layer overlying the at least one via opening to form at least one via plug;

forming a photoresist layer over the DARC layer for photolithographically patterning a trench line opening disposed substantially over the at least one via opening;

photolithographically forming a trench line opening disposed substantially over the at least one via opening to expose a portion of the DARC layer forming a trench line pattern;

anisotropically etching according to the trench line pattern through at least a thickness of the DARC layer and hard mask layer to include a portion of the at least one via plug; and

anisotropically etching according to the trench line pattern through a portion of a thickness of the insulating layer to form a trench line opening disposed substantially over a remaining portion of the at least one via opening.

2. The method of claim 1, wherein the insulating layer has a dielectric constant of less than about 3.0.

3. The method of claim 2, wherein the insulating layer comprises an interconnecting porous material.

4. The method of claim 2, wherein the insulating layer comprises carbon doped oxide.

5. The method of claim 1, wherein the hard mask layer and DARC layer comprise a metal nitride.

6. The method of claim 3, wherein the metal nitride is selected from the group consisting of silicon nitride, silicon oxynitride and titanium nitride.

7. The method of claim 4, wherein the metal nitride is deposited according to a chemical vapor deposition process.

8. The method of claim 1, wherein the resinous layer comprises a photoresist resin flowable at room temperature.

9. The method of claim 1, wherein the step of anisotropically etching through a thickness of the DARC layer and hard mask layer to include a portion of the via plug further comprises reactive ion etching (RIE) with an etching chemistry whereby the etching selectivity of the via plug to the hard mask is greater than about 1.

10. The method of claim 1, wherein the step of anisotropically etching through a thickness of the DARC layer and hard mask layer to include a portion of the via plug further comprises reactive ion etching (RIE) with a nitrogen and oxygen containing plasma having a nitrogen to oxygen ratio of at least about 5.

11. The method of claim 9, said plasma further including hydrogen.

12. The method of claim 1, further comprising an ashing and cleaning process following the step of anisotropically etching through the insulating layer to form a trench line.

13. A method for preventing the occurrence of undeveloped photoresist in semiconductor manufacturing process comprising the steps of:

providing an anisotropically etched first opening extending through a thickness of layers sequentially including at least one metal nitride layer and an insulating layer;

forming a resinous layer over the at least one metal nitride layer to include filling the first opening;

removing the resinous layer overlying the etched opening to form a plug filling the first opening;

forming a photoresist layer over the at least one metal nitride layer for lithographically patterning a second opening disposed over the first opening;

lithographically patterning a second opening disposed over the first opening to expose a portion of the at least one metal nitride layer forming an etching pattern;

anisotropically etching according to the etching pattern through at least a thickness of the at least one metal nitride layer to include at least a portion of the plug; and

anisotropically etching according to the etching pattern through a thickness portion the insulating layer to form the second opening and a remaining portion of the first opening said second opening disposed substantially over the remaining portion of the first opening.

14. The method of claim 13, wherein the insulating layer has a dielectric constant of less than about 3.0.

15. The method of claim 14, wherein the insulating layer comprises an porous material including interconnecting pores.

16. The method of claim 14, wherein the insulating layer comprises carbon doped oxide.

17. The method of claim 13, wherein the at least one metal nitride includes at least one of silicon nitride, silicon oxynitride and titanium nitride.

18. The method of claim 13, wherein the resinous layer comprises a photoresist.

19. The method of claim 13, wherein the step of anisotropically etching through at least a thickness of the at least one metal nitride layer to include at least a portion of the plug further comprises reactive ion etching (RIE) with an etching chemistry whereby the etching selectivity of the via plug to the hard mask is greater than about 1.

20. The method of claim 13, wherein the lithographic process is deep ultraviolet (DUV) process.